UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,135	03/17/2000	Tohru Watanabe	005586-20035	5243

26021 7590 10/05/2005

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
MISLEH, JUSTIN P	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/531,135	WATANABE, TOHRU	
	Examiner	Art Unit	
	Justin P. Misleh	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2 - 6 and 8 -10* is/are allowed.

6)☒ Claim(s) *1,7 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/29/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed July 14, 2005 have been fully considered but they are not persuasive. However, Applicant's amendment to Figure 3 overcomes the previous objection; there are no further objections.

2. Applicant argues, "the reference [Yamanka et al.] does not describe a means corresponding to the 'timing control circuit' of the present invention 'for setting a storage time of information charges at the first light receiving pixel and a storage time of information charges at the second light receiving pixel.'"

The Examiner disagrees with Applicant's position. Yamanka et al. clearly teach the above-recited feature in column 7 (lines 50 – 57). More specifically, Yamanka et al. states, "The reading of the stored charges is performed by a control pulse from the CCD driver circuit 18 ... it is only needed to change the timing of the storing or reading by the control pulse, whereby the charge storage time can be varied to adjust the exposure." Furthermore, Yamanka et al. indicates, in column 7 (lines 40 – 49), "As shown in FIG. 4(A), as the field O (Odd)/E (Even) signal, a timing signal for forming one field in 1/60 sec is used as in the conventional system. In response to this, by causing the light chopper 36 to make one turn in 1/30 sec, light is repetitively outputted with a period of 1/60 sec while interlacing with light intercepted states of 1/60 sec, as shown by Pn-1, Pn, and Pn+1 of FIG. 4(B)." Therefore, Yamanka et al. disclose respectively setting the storage time (1/60 second) of information charges at the first light receiving pixel

(EVEN) and the storage time (also 1/60 second) of information charges at the second light receiving pixel (ODD), as recited by the claim language.

3. Applicant makes comments/arguments regarding Yonemoto, which was listed on form PTO-892 (mailed April 20, 2005).

Yonemoto was not applied in claim rejections; hence, Applicant's arguments are moot.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1, 7, and 11** are rejected under 35 U.S.C. 102(e) as being anticipated by Yamanaka et al.

6. For **Claim 1**, Yamanaka et al. disclose, as shown in figures 1, 2, and 4 and as stated in columns 6 (lines 16 – 67), a solid-state image pickup apparatus (see figure 1) comprising:

a solid-state image pickup device (11) in which a first light receiving pixel (EVEN) is disposed in a plurality of lines in one-line units (see figure 2A), and a second light receiving pixel (ODD) capable of being driven independently (see figures 2B, 2C, and 4 and column 6, lines 18 – 26) from said first light receiving pixel (EVEN) is disposed in at least one-line units between first light receiving pixels of the plurality of lines (see figure 2A);

a drive circuit (18; see figure 1) for driving the first and second light receiving pixels (EVEN and ODD) of said solid-state image pickup device (11) and accumulating information charges at mutually different times (see figures 4A and 4C) between first light receiving pixel (EVEN) and second light receiving pixel (ODD), as well as transferring and outputting information charges accumulated in said first and second light receiving pixels independently of each other (see figure 4C);

timing control circuit (20; see figure 1) for respectively setting the storage time of information charges at the first light receiving pixel (EVEN) and the storage time of information charges at the second light receiving pixel (ODD) of said solid-state image pickup device (1); and

a signal processing circuit (24; see figure 1) for generating an image signal by adding a first output corresponding to the first light receiving pixel and a second output corresponding to the second light receiving pixel of said solid-state image pickup device (see figures 2D, 2E, and 4G);

wherein after driving the first and second light receiving pixels (EVEN and ODD) to accumulate information charges in the first and second light receiving pixels (EVEN and ODD), the drive circuit (18; see figure 1) adds information charges accumulated in the first light receiving pixel (EVEN) to information charges accumulated in the second light receiving pixel (ODD), and, the drive circuit drives the first and second light receiving pixels to further accumulate information charges in the first and second light receiving pixels and further adds information charges thus accumulated in the first and second light receiving pixels (see figures 2D and 2E and also see column 3, lines 17 – 33, and column 8, lines 17 – 22).

7. For **Claim 7**, a solid-state image pickup apparatus (see figure 1) comprising:

a solid-state image pickup device (11) having a line of first light receiving pixels (EVEN) and a line of second light receiving pixels (ODD) disposed so as to respectively correspond to horizontal scanning lines (see figure 2) and capable of being driven independently (see figures 2B, 2C, and 4 and column 6, lines 18 – 26) from each other said first light receiving pixels (EVEN) and said second light receiving pixels (ODD);

a drive circuit (18; see figure 1) for driving the first and second light receiving pixels (EVEN and ODD) of said solid-state image pickup device (11) and accumulating information charges at mutually different times (see figures 4A and 4C) between first light receiving pixel (EVEN) and second light receiving pixel (ODD), as well as transferring and outputting information charges accumulated in said first and second light receiving pixels independently of each other (see figure 4C) and generating a first output according to said information charges accumulated in said first light receiving pixels (see figure 4D) and a second output according to said information charges accumulated in said second light receiving pixels (see figure 4D); and

a signal processing circuit (24; see figure 1) for generating an image signal by adding together the first output and the second output corresponding to identical horizontal scanning lines (see figures 2D, 2E, and 4G);

wherein after driving the first and second light receiving pixels (EVEN and ODD) to accumulate information charges in the first and second light receiving pixels (EVEN and ODD), the drive circuit (18; see figure 1) adds information charges accumulated in the first light receiving pixel (EVEN) to information charges accumulated in the second light receiving pixel (ODD), and, the drive circuit drives the first and second light receiving pixels to further

accumulate information charges in the first and second light receiving pixels and further adds information charges thus accumulated in the first and second light receiving pixels (see figures 2D and 2E and also see column 3, lines 17 – 33, and column 8, lines 17 – 22). (see figures 2D and 2E).

8. For **Claim 11**, Yamanaka et al. disclose, as shown in figures 1, 2, and 4 and as stated in columns 6 (lines 16 – 67), a solid-state image pickup apparatus (see figure 1) comprising:

a solid-state image pickup device (11) in which a first light receiving pixel (EVEN) is disposed in a plurality of lines in one-line units (see figure 2A), and a second light receiving pixel (ODD) capable of being driven independently (see figures 2B, 2C, and 4 and column 6, lines 18 – 26) from said first light receiving pixel (EVEN) is disposed in at least one-line units between first light receiving pixels of the plurality of lines (see figure 2A);

a drive circuit (18; see figure 1) for driving the first and second light receiving pixels (EVEN and ODD) of said solid-state image pickup device (11) and accumulating information charges at mutually different times (see figures 4A and 4C) between first light receiving pixel (EVEN) and second light receiving pixel (ODD);

timing control circuit (20; see figure 1) for respectively setting the storage time of information charges at the first light receiving pixel (EVEN) and the storage time of information charges at the second light receiving pixel (ODD) of said solid-state image pickup device (1); wherein

after driving the first and second light receiving pixels (EVEN and ODD) to accumulate information charges in the first and second light receiving pixels (EVEN and ODD), the drive circuit (18; see figure 1) adds information charges accumulated in the first light receiving pixel

(EVEN) to information charges accumulated in the second light receiving pixel (ODD), and, the drive circuit drives the first and second light receiving pixels to further accumulate information charges in the first and second light receiving pixels and further adds information charges thus accumulated in the first and second light receiving pixels (see figures 2D and 2E and also see column 3, lines 17 – 33, and column 8, lines 17 – 22).

Allowable Subject Matter

9. **Claims 2 – 6 and 8 – 10** are allowed.

10. The following is a statement of reasons for the indication of allowable subject matter:

While the closest prior art (Yamanka et al. and Yonemto) discuss the particulars of the solid-state image pickup apparatus including first and second light receiving pixels, the independent accumulation of charge in the first and second light receiving pixels, the independent storage of charge of the accumulated first and second light receiving pixels, and the summing of the stored and accumulated charge of the first and second light receiving pixels, as required and discussed above in regards to Claims 1, 7 and 11;

The closest prior art does not teach or fairly suggest calculating a vertical transfer smear component on the basis of a ratio of said respective accumulation times of information charges at said first and second light receiving pixels and of a difference of said first and second outputs corresponding to said first and second light receiving pixels; does not teach or fairly suggest calculating a smear quantity generated during vertical transfer of said information charges on the basis of a ratio of said respective accumulation times of said information charges at said first and second light receiving pixels and of said first output and said second output; and does not teach

or fairly suggest calculating smear quantity generated during vertical transfer of said information charges on the basis of a ratio of said respective accumulation times of said information charges at said first and second light receiving pixels and of said first output and said second output.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Ngoc Yen Vu can be reached on 571.272.7320. The fax phone number for the organization where this application or proceeding is assigned is 571.273.3000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
September 29, 2005

NGOC-YEN VU
PRIMARY EXAMINER

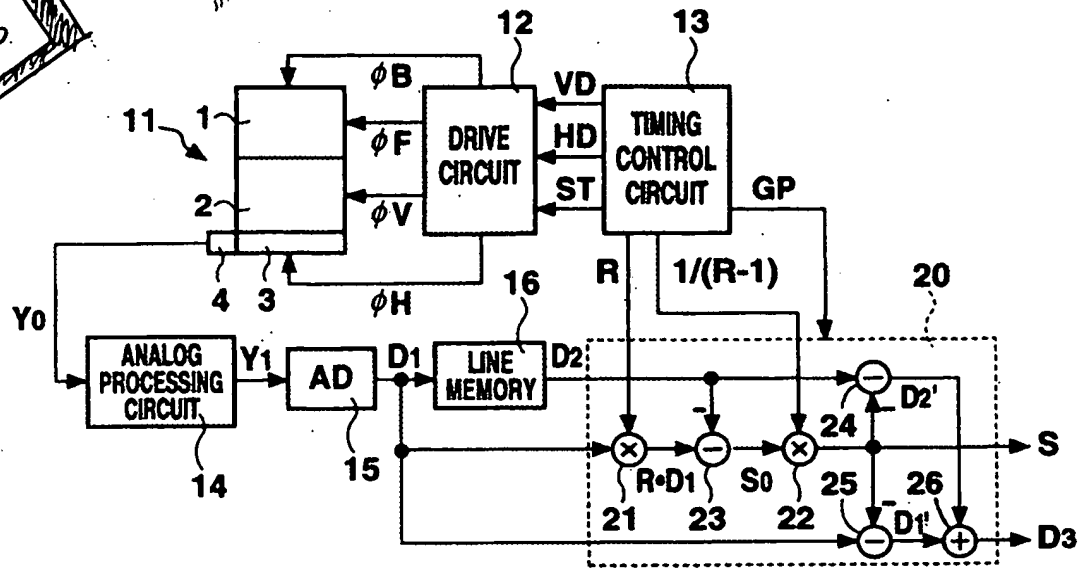

Fig. 3

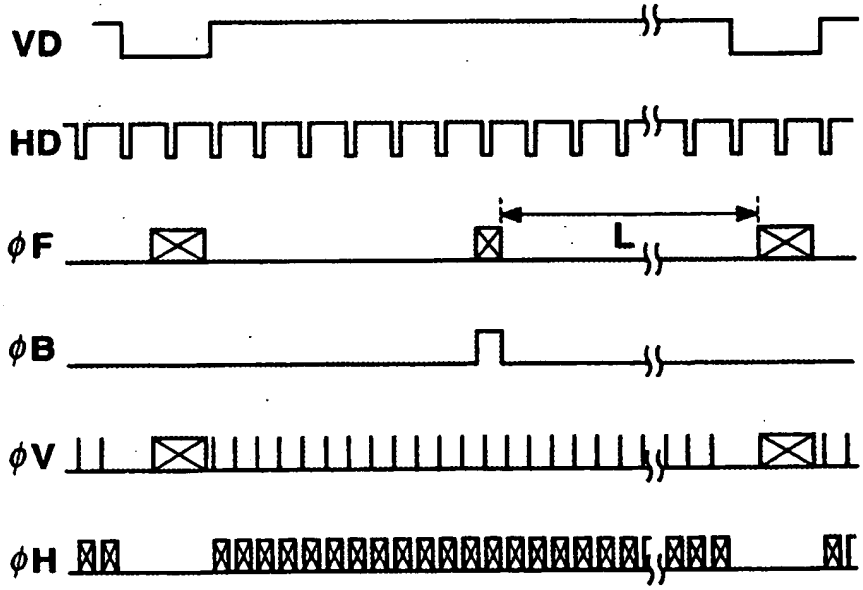

Fig. 4